REMARKS

In response to the Office Action mailed on March 14, 2006, Applicant wishes to enter the following remarks for the Examiner's consideration.

Applicant has submitted three Replacement Sheet Drawings to replace the informal drawings with the formal drawings.

Applicant has amended claims 1 and 9-15 and added new claims 24-31. Claims 1-31 are pending in the application.

Rejection of claims under 35 USC §102(b)

Claims 1-5, 9-10, 15-17 and 21-22 have been rejected under 35 USC §102(b) as being anticipated by Watkins, US Patent No. US 5,937,436. Applicant respectfully traverses this rejection of the claims in view of the amendments to claims 1 and 15.

Claim 1 has been amended to clarify that both interfaces of the address translation filter operate under the same bus protocol. This amendment makes explicit meaning that was previously in the claim. As originally drafted, claim 1 referred to a (single) system bus and is it inherent that a single bus does operate under two protocols simultaneously. This change is supported by the specification on page 5, lines 3-8. In addition, original claim 14 referred to a filter in which the system bus operated under a single protocol (either AMBA or AHB protocol). The address translation filter of claim 1 is for filtering a signal on a system bus.

In contrast, Watkins discloses devices for translating one bus protocol to a different bus protocol. Applicant submits that operations of filtering and protocol conversion are not equivalent. In particular, the specification on page

5, lines 4-5, states that a filter is not required to perform protocol translation. Watkins figure 2a shows a number of interfaces to the system bus 230 (e.g. CPU's 210_i, and the interfaces to the memory 230 and the bridge 240. However, there are no elements connected between any of these interfaces. The bridge 240 has two interfaces and connects between the system bus 230 and the I/O bus 270. However in claim 1, as amended, the first and second interfaces are both interfaces operable to couple to system bus under the same protocol. The Network Interface Circuit 260_k in figures 2a and figure 4 is coupled between an I/O bus 270 and at ATM interface 320. These operate under different protocols and the function of the NIC is to translate between the protocols. Similarly, bridge 240 provides protocol translation between the system bus 230 and I/O bus 270, which operate under different protocols.

In contrast to the address translation filter of claim 1, the I/O bus 270 does not couple between a core processor and an external memory unit, as is called for in claim 1.

The examiner opines that network media 320 is a bus of the system and therefore a system bus. However, a system bus is link between components in a system whereas network media 320 is a link between disparate systems. Further, claim 1 defines the system bus as coupling the CPU to the main memory.

In an interview on March 11th, 2006, the examiner agreed that the Watkins reference did not disclose an address translation filter that both received and transmitted bus signals in accordance with a single bus protocol.

Claims 2-5 depend from claim 1. Although additional arguments could be made for the patentability of claims 2-5, such arguments are believed

unnecessary in view of the above discussion.

Claim 9 has been amended to explicitly call for the system bus linking the core processor the external memory to operate under the same bus protocol as the system bus linking the external processing device to the address translation filter. This element, which was inherent in the claim before amendment, is supported by the specification on page 5, lines 3-8, and by original claim 14. This feature of the claim is not disclosed by the Watkins reference.

Claim 9 has been further amended to specify that the digital processing system is an integrated circuit. This amendment is supported by the specification on page 1, lines 9-20 and page 5, lines 12-17 (AMBA is an on-chip bus specification) and by original claim 14. The interface circuit 260 of the Watkins reference provides a connection between physically disparate systems. The Watkins reference does not disclose an integrated circuit that includes the elements of claim 9.

Claim 9 also calls for the address translation unit to be operable to translate a virtual memory address received *via the system* bus from the external processing device into a physical memory address that is transmitted *via the system bus* to the external memory unit. Thus, the address translation unit acts as a filter on the system bus. The address translation unit receives a signal from the bus as input and provides a signal to the bus as output. This is in contrast to Figure 4 of Watkins, which shows an address translation unit 450 in an address generation unit 440. Watkins' address generation unit provides an interface between the I/O bus 270 and an ATM core. The ATM core is not equivalent to a system bus. Watkins' address generation unit 440

is indirectly coupled to the ATM network medium 320, by the ATM network medium operates under a different protocol to the I/O bus. Applicant submits therefore that Watkins does not teach a filter on a system bus.

In an interview on March 11th, 2006, the examiner agreed that the Watkins reference did not disclose an address translation filter that both received and transmitted bus signals in accordance with a single bus protocol.

Claim 10 depends from claim 9. Although additional arguments could be made for the patentability of claim 10, such arguments are believed unnecessary in view of the above discussion.

Claim 15 was previously amended to clarify the first bus signal is received from a bus and that the second bus signal is transmitted to the same bus. Claim 15 has been further amended to clarify that the first bus signal received from a device via the bus and the second bus signal transmitted via the bus to the external memory unit use the same bus protocol. This is not taught by Watkins. Watkins teaches the use of an address translation unit 450, but he does not teach that the address translation unit operates as a filter on a bus. Figure 4 of the Watkins reference shows an address translation unit 450 in an address generation unit 440. The address generation unit provides an interface between the I/O bus 270 and an ATM core. It does not receive a bus signal from the bus, translating a virtual memory address specified by the bus signal to a physical memory address in an address translation filter, and then transmit a bus signal to the bus in accordance with the physical memory address, as called for by claim 15. Rather, the signals are received by the address generation unit 440 from the ATM network medium 320 via the ATM core using an ATM protocol and then transmitted to the bus 270 using a

different protocol (such as a PCI protocol, column 3, lines 49-54).

Claims 16-17 and 21-22 depend from claim 15. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion.

In light of the foregoing amendment and remarks, Applicant respectfully submits that the Watkins reference does not teach, suggest, disclose or otherwise anticipate the recitations of claims 1-5, 9-10, 15-17 and 21-22. Applicant thus respectfully requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

Rejection of claims under 35 USC §103(a)

Claims 7, 14, 20 and 23 have been rejected under 35 USC §103(a) as being unpatentable over Watkins, US Patent No. U.S. 5,937,436. Applicant respectfully traverses this rejection of the claims in view of the amendments to claims 1 and 15.

Claim 7 depends from claim 1. As discussed above, claim 1 has been amended to clarify that the first and second interfaces of the address translation operate under the same bus protocol. This element was previously inherent in the claims since the address translation filter was described as operating as a filter on a system bus. The examiner has opined that system bus 230, I/O bus 270 and ATM link 320 in the Watkins reference are all buses of the system. However, Applicant submits that they are not a bus of the system, nor are they a system bus. Watkins discloses a

networking interface circuit NIC) that operates between an I/O bus and an ATM core (see figures 3 and 4 and the associated description thereof). The objective of the NIC is to add address translation to an interface that translates between different protocols (the I/O bus protocol and the ATM protocol). The Watkins reference does not to motivate one of ordinary skill in the art to consider a bus filter. A bus filter as claimed in claim 1 and dependent claim 7 receives a signal from the bus as input in accordance with one bus protocol and provides a signal to the same bus as output in accordance with the same bus protocol. No protocol translation is required since the input and output operate under the same protocol.

The applicant submits that is would not be obvious for one of ordinary skill in the art for the address translation filter to both receive and transmit a system clock signal, as called for in claim 7.

Claim 14 has been written in independent form to include all of the limitations of original claim 9. Claim 14 calls for the bus to be either an ABMA or an AHB. This indicates that the bus has a single protocol and therefore the protocol is the same on both sides of the address translation filter. Watkins does not teach of otherwise suggest that the protocol is the same on both sides of the address translation filter 450. Further, Watkins teaches only interfaces between physically disparate systems. In contrast, ABMA or an AHB are buses for communication between elements (blocks) on an integrated circuit. Applicant submits that there is nothing in Watkins to such the use of a single bus protocol, or that an 'on-chip' protocol, such as the AMBA, should be used.

Claims 20 and 23 depend from claim 15 discussed above. Claim 15

been amended to clarify the first bus signal is received from a bus and that the second bus signal is transmitted to the same bus. This distinguishes the claim from the NIC disclosed by Watkins, since the Watkins reference discloses an interface between dissimilar protocols, and does not teach, disclose or otherwise suggest the use of a bus filter operating on a single bus. Claim 15 has been further amended to clarify that the bus couples between a core processor and the external memory unit. Referring to figure 2a of the Watkins reference, the NIC operates between the I/O bus 270 and an ATM core, while the bridge interfaces between dissimilar bus architectures (230 and 270).

Regarding claim 23, transferring an initial memory map to an internal device, such as 112 in Figures 1 and 2 of the application, is not equivalent to transferring an initial memory map to an external address translation filter 118.

Claims 6, 8, 11-13 and 18-19 have been rejected under 35 USC §103(a) as being unpatentable over Watkins, US Patent No. US 5,937,436 in view of McGrath, US Patent No. 6,671,791. Applicant respectfully traverses this rejection of the claims in view of the amendments to claims 1, 9 and 15.

The Examiner acknowledges that the Watkins reference fails to teach, disclose or suggest the recitation of the claims, and relies upon the teachings of McGrath to overcome this defect. As discussed above with reference to independent claims 1, 9 and 15 from which claims 6, 8, 11-13 and 18-19 depend, Watkins does not teach, disclose or suggest the use of a filter on a bus. Instead, he teaches an interface to a bus and a bridge between dissimilar buses. In addition to this, the Examiner acknowledges that the

Watkins reference fails to teach, disclose or suggest the use of an output control link, and relies upon the teachings of McGrath to overcome this defect.

Referring to figure 3 of the McGrath reference, the MMU 20 is integral to a processor 10 and communicates with an execution core 14 that is also integral to the processor 10. The function of the MMU 20 is similar to that of the virtual to physical memory map 112 shown in Figures 1 and 2 of the application. In particular, the MMU does not lie on the system bus between a core processor and an external memory unit, as is called for in claims 1 and 15. Further, the MMU 20 is not external to the processor 10. The MMU 20 is not accessible to external devices (such 114 and 116 in Figure 2 of the application) that are coupled to the bus structure. This forces these devices to address the external memory using physical addresses and complicates the programming of the devices.

McGrath teaches signaling between the execution core and an MMU that is integral to processor 10, but does not teach signaling between a core processor and an external address translation filter.

In light of the foregoing remarks, Applicant respectfully submits that the Watkins and McGrath references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim 6, 8, 11-13 and 18-19. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 6, 8, 11-13 and 18-19 be mailed at the Examiner's earliest convenience.

New Claims

Applicant has added new claim 24-31. New claims 24-28 are similar in scope to original claim 14-18, but depend from the amended claim 9. The amendment to claim 9 has been discussed above. No new material has been added.

New claims 29-31 relate to a digital processing circuit in which an address translation filter is operable to couple a processing device to the system bus under the same system bus protocol that links a core processor to an external memory unit. As discussed in the remarks above, the Watkins reference only discloses an address translation unit that operates between different bus protocols. Further the Watkins reference only discloses interfaces between physical disparate elements. In contrast, the elements of claim 29 occupy the same digital processing circuit. Further, claim 30 calls for the core processor, the address translation filter and the processing device to occupy the same integrated circuit.

Support for the elements being in a single digital circuit is provided by the specification on page 1, lines 9-20 and page 5, lines 12-17 (AMBA is an on-chip bus architecture specification) and original claim 14 (which again referred to an AMBA).

In light of the foregoing amendments and explanations, applicant submits that all rejections of claims 1-23 have been overcome. The scope of the amended claim 1 is substantially the same with implicit meaning now made explicit. Scope of rewritten claim 14 is as originally filed. Allowance of claims 1-31 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of

the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,

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